

RMV ELECTRONICS INC.

Application Note

Application note #: 24

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Title: SIGNAL CONDITIONING FOR THE I/O-232 AND I/O-485 DATA ACQUISITION BOARDS

Status: Final

Some of our boards use an eleven channel analog/digital converter (ADC), with a resolution of 8, 10 or 12 bits. These ADC's are designed to read voltages against a reference which is recommended to be above 2 Volts. As a result, it is often necessary to amplify or change the offset of a signal (conditioning) which might be originally in the mV or μ V range. The following examples show how to address some very common situations:

1.a Reading resistive devices

A resistance can be read using an ADC and a voltage dividing resistor network. The ITC232-A, can however, read a resistor in an RC network. This is thoroughly explained in the ITC232-A User Guide. (This is just a reminder that such a feature exists and that the 4 lower pins of PC in that chip can be used for this purpose (and for reading capacitance too)).

1.b Reading a current

Some devices such as photovoltaic cells and thermocouples can be better considered as current sources rather than voltage sources. Thus, before reading the output of any such device, a current to voltage conversion is required. The circuit in Figure 1 shows the classical way to do this.

As you can notice, an inverting configuration must be used and this means that a double voltage power supply is required. This is not always practical. There is a way around this problem and that is shown in Figure 2:

An artificial ground is created by R4 and R5. The values are unimportant and even though it is recommendable that they are similar they do not need to be closed matched. The current source is placed between the artificial ground and the inverting input. Thus, the output of the first op amp will range between $VCC / 2$ and some voltage closer to one of the rails (VCC or GND). A second op amp is used to invert the signal back to normal as we did before. The current source can also be inverted and therefore the 2nd op amp becomes unnecessary.

1.c Converting a +5V to -5V signal into a 0 to 5 Volt signal

Some commercial devices produce voltage outputs ranging from -5 to +5 Volts. The ADC in our I/O line of boards can read voltages from 0 to +5 Volts. Thus, either a differential ADC must be used or a signal conditioning circuit must be used. We will discuss here the latter.

The solution to the problem is to connect 2 resistors (R1 and R2) of identical value to each ADC input as shown in Figure 3. The other end of R1 goes to +5V (Vbias) and the other end of R2 goes to the input signal. The value of the resistors is not critical provided that (a) they are as well matched as possible, (b) they are compatible with the output impedance of the signal source and (c) the value does not exceed 10 K (as recommended by the ADC manufacturer). Values between 1K and 10K are recommended.

Since both resistors are equal, the voltage drop introduced by each one is 1/2 of the total voltage drop and therefore, the voltage at the joining point(Vj), which is where the ADC is connected, equals $(V_{bias} + V_{in}) / 2$. Since R1 is connected to +5V then $V_{bias} = +5$.

If $V_{in} = -5V$, then $V_j = (+5 + -5) / 2 = 0$ Volts.
If $V_{in} = +5V$ then $V_j = (+5 + +5) / 2 = 5$ Volts.

Each Volt at the input results in 0.5 Volts at the joining point of the resistor network, in the 0 to +5 Volts.

1.d Amplifying a single polarity small signal to a 0-5 Volt range

Figure 4 shows how to use an operational amplifier to address this situation. It is important to use a high quality op-amp such as the OP-05 from TI. It is also highly desirable that its output can swings from rail to rail in order to avoid flattening of the curve of response as the output reaches values close to 0 or VCC.

The output of this circuit can be calculated using $V_{out} = V_{in} * (1 + R1 / R2)$

1.e Amplifying a double polarity small signal to a 0-5 Volt range

Figure 5 is a combination of the circuits discussed in 1.c and 1.d with a twist. This circuit has the advantage over the one in Figure 3 that the input resistances (R) can now be higher than 10K since the inputs are buffered from the ADC by the op amp. Again, the value of these 2 resistors must be matched as closely as possible.

U1a creates a positive bias which must be equivalent to the maximal negative value of the input. That bias voltage (V_{bias}) must be measured on the output of U1a. The bias offsets the input voltage the same way as it was described in 1.a. The resulting voltage is then applied to the non-inverting input of U1b which is configured as a non-inverting amplifier. The output voltage can be calculated using $V_{out} = (V_{in} + V_{bias}) / 2 * (1 + R1 / R2)$.

Should you have the maximal value produced by the device being read (V_{inmax}) and the maximal value the ADC can read (which can be varied using the trimmer connected to V_{ref} on the ADC and referred to as V_{outmax}), the following equation can be used:

$R1/R2 = (V_{outmax} / (V_{inmax} + V_{bias}) / 2) - 1$ (some of the brackets are inserted for clarity purposes).

Example: Your device produces a - 10 mV to + 5 mV and the V_{ref} on the ADC is set to 3 V.

V_{outmax} is then +3, $V_{inmax} = +0.005$ and $V_{bias} = +0.010$

$(V_{inmax} + V_{bias}) / 2 = 0.0075$

$V_{outmax} / 0.0075 = 3 / 0.0075 = 400$

$R1/R2 = 400 - 1 = 399$

$R1$ could be then 399K and $R2 = 1K$

If you use these values in the equation above you will get 3 V for a V_{in} of +5 mV and 0 for a V_{in} of -10 mV.
 $V_{in} = 0$ will yield 2 V output.

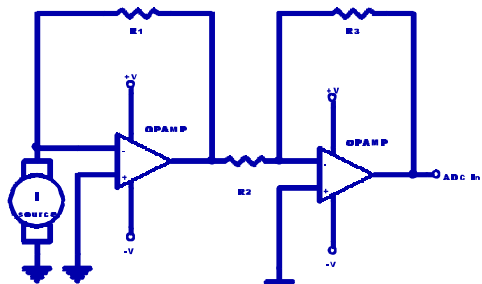


Figure 1

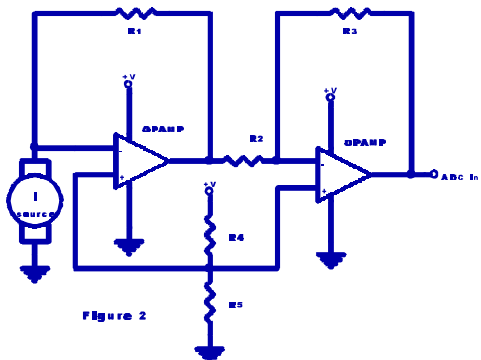


Figure 2



Figure 3

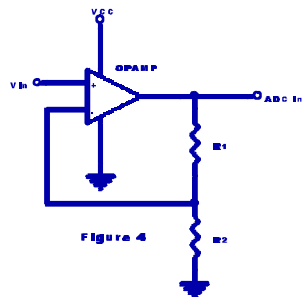


Figure 4

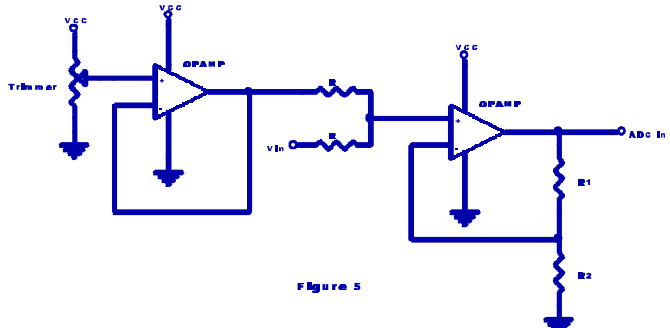


Figure 5

